

12 Pages

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can en-charge to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in answer book and cross it through.
6. No part of this book is to be torn out; it must be handed complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. **Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.**

1	Student Number	2502815
2	Title of Examination Paper	Computer Architecture and Operating Systems
3	Module Code	ACC4022
4	Date and Time of Examination	11/5/2026
5	Examination Venue	3/0
6	Seat Number	23
7	Number of Answer Books handed in	1

List the numbers of the questions you have attempted	Office Use
1	24
2	11
3	16
4	07
Total	58

(Gweler yr ochr arall am y fersiwn Cymraeg)

lated to the CPU to
other parts too;
to interpret how

1)

- (a) The importance of numbersystems is highly related to the CPU to understand the human language and ~~for~~ for the other parts too; ~~which~~ which each numbering system has its own way to interpret how the ~~PC~~ PC will process.

(b) 256 128 64 32 16 8 4 2 1

i 0 1 1 1 1 0 1 0 1

~~245~~ = 1111 0101

512 256 128 64 32 16 8 4 2 1

ii 1 0 0 0 0 0 0 0 0 0

512 = 0010 0000 0000

(c) 128 64 32 16 8 4 2 1

1 1 0 1 0 1 0 1

i 128 + 64 + 16 + 4 + 1

ii = 213

256 128 64 32 16 8 4 2 1

1 0 1 0 1 1 0 0 1

ii 256 + 64 + 16 + 8 + 1

ii = 345

(d) E A B
14 10 11
8421 8421 8421

i 1110 1010 1011

ii = EAB

ii 1001 1111 0010

ii = 962

(e) 256 128 64 32 16 8 4 2 1

i C3 = 1100 1011

C3 = 203

ii 66 = 0110 0110

66 = 102

1

f

~~$3^2 = 9$~~

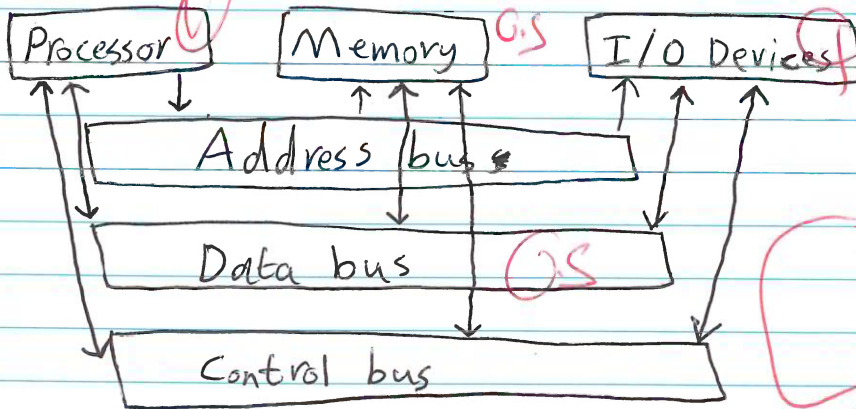
9

$36/8 = 4.5$

$80/4.5 \approx 17.8$ seconds

2) a)

Harvard Computer architecture



- ⑥ Cache memory and registers are high speed temporary memory and can store the emergency or important data needed by the CPU, ~~it~~ ~~not~~ so it can help the CPU to process operations faster.

11/25

6 [7/13]

3\

① Secondary memory is an additional memory to ~~bypass~~ the CPU's bottleneck.

HDD	SSD
1- Very cheap.	1- Can be expensive.
2- Slow.	2- Very fast.

② RAID 0\

- 1- Data is segmented in 2 drives.
- 2- If a drive fails, ~~the~~ data will be lost.

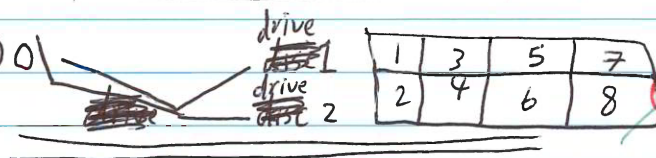
RAID 1\

- 1- Data is stored in ~~2~~ drives in parallel.
- 2- Easier for backups if a drive fails.

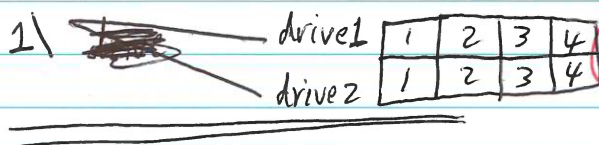
RAID 10\

- 1- ~~At least~~ many drives needed to store the data.
- 2- The data is stored in segmented and parallel way.

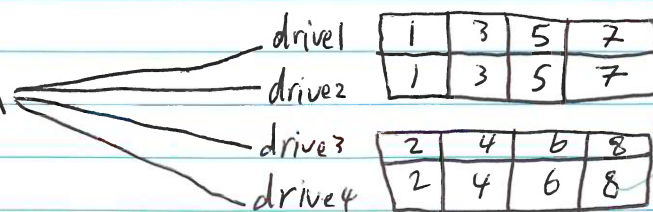
③ RAID 0\



RAID 1\



RAID 10\



④ RAID 0\

- 1- Easy to setup.

- 2- Hard to backup if a drive fails.

RAID 1\

- 1- Easy to backup.

- 2- More prone to viruses even after backup.

RAID 10\

- 1- Can be very fast.

- 2- High cost (at least 4 drives).

4 a

Fetch-Decode-Execute cycle

→ CPU waits instructions from memory → PC sends ^{Addresses} ~~addresses~~ to memory
 memory sends Address to MDR - MAR to MDR - MDR to IR
 IR to ALU to do ^{calculations} ~~calculations~~ or operations by using Op codes and operands → to memory

- ⑥ 1- Fetch \ - The program counter sends the instruction addresses to memory.
- The memory sends the addresses to [memory address register].
 - The instruction is copied to the [memory data register].
 - The instruction is moved to the [Instruction register].

2- DeCode \

- The IR moves the ~~the~~ instruction to the [Arithmetic logic unit]
- It determines the op codes and operands to regulate the instructions in ~~memory~~ registers or memory located.

3- Execute \

- The PC executes the ~~the~~ instructions unless there are jumps or branches.
- It waits ^{or} adds the next instruction.

MAR \ → to store instruction Addresses.

MDR \ moves instructions to IR

IR \ stores the instructions ~~and~~

ALU \ to do arithmetic and logic operations.

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